FIBERBLAZE
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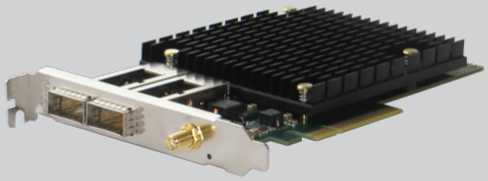


fbSmartNIC1.0 for time critical communication

The fbSmartNIC2.0 product is designed to competitively enhance performance in a host of networking, financial and big data solutions. It consists of highly optimised functionality well suited for e.g. financial algorithmic trading platforms where sub-micro second latency is crucial.

Complete transport layer offload can be combined with customised logic directly implemented in the powerfull on board FPGA. It comes with a full Software API for a seamless integration and monitoring. It is available on stock from Fiberblaze.

HOST INTERFACE
- Physical bus connector: 8-lane PCIe
- Supported bus type: 1-8 lane PCIe Gen3, Gen2 & Gen1
- PCIe compliant

TIME STAMPING & SYNC
- External synchronization: PPS
- Daisy chain between multiple cards supported

NETWORK INTERFACE
- IEEE standard: IEEE 802.3 10 GbE
- Physical interface: 2 x QSFP+ ports
- Supported QSFP+ modules: Including fan out modules for 4 x 10G, multimode SR (850 nm), singlemode LR (1310 nm), multimode LRM (1310 nm), or Direct Attached Copper (Twinax)
- Data rate: 8 x 10 Gbit/s
- Ethernet PHY directly embedded in FPGA

CONFIGURATION
- 16 bit parallel master interface from supporting pre-programmed Actel FPGA
- Configuration flash supports two boot images with automatic fallback to fail safe image if first image fails
- Upload of FPGA configuration to flash via PCIe
- Upload of FPGA configuration to flash via USB

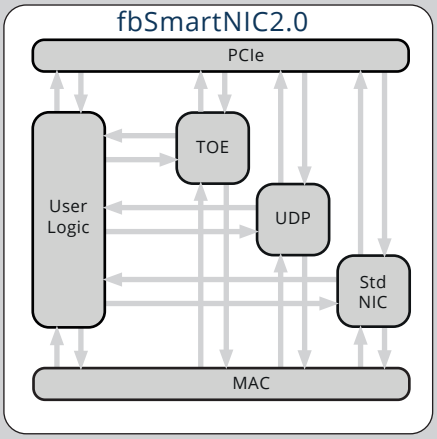
ON BOARD MEMORY
- 2 x 64 bit DDR3@1600MT/s 4GB (total 8GB memory)

ON BOARD CLOCK
- 125.00 MHz oscillator
- 156.25 MHz oscillator

FPGA VERSION
- Xilinx Virtex7 XC7VX690T

ENVIRONMENT
- Physical characteristics: Half length, standard height PCIe: 111 x 169 mm. Weight: 129 g.
- Power consumption: Less than 25W
- Operating temperature: 0 – 55°C, 30 – 130°F
- Operating humidity: 20 – 80%
- Hardware compliance: RoHS, CE

ADDITIONAL BOARD SUPPORT
- On board temperature sensor
- Pre-programmed Atmel CPU with power measurement, host SMB I/F, USB I/F
- Board status LED
- FPGA controlled Link and Activity LED for each port
- External clock synchronization connector



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Dedication to Performance

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fbSmartNIC1.0 Framework

The fbSmartNIC framework is designed to enhance performance in a host of networking, financial and big data scenarios. Key benefits include increased throughput with zero data loss without interruption of server processes. Business opportunities such as e.g. High Frequency Trading and High Volume Data Collection systems can benefit substantially from this complete hardware off-loading of TCP/UDP communication. It includes market leading TOE (TCP Offload Engine) and UOE (UDP Offload Engine) as well as a highly optimised MAC layer. The fbSmartNIC framework supports various Fiberblaze cards featuring technologies such as Xilinx, Altera and ZYNQ.

HOST INTERFACE
- 64 logical channels connected to DMA

LATENCY
- Wire to wire latency of 345 ns: Receiving on UDP port, through User Logic, and sending from TCP port
- Full 10G throughput on TCP port

MAC
- Combined MAC (10GbE) and PCS (10GBASE-R) IP core
- Fixed latency of 101 ns: User Logic to wire, Tx + Rx

PERFORMANCE
- Data rate: 10 Gbit/s
- TCP/UDP throughput at line rate

TIME STAMPING & SYNC
- Resolution = 1ns
- Accuracy down to 20 ns

ENVIRONMENT
- At least half of the FPGA resources are available for User Logic

UDP OFFLOAD ENGINE
- 64 UDP multicast streams accessible to Host and User Logic
- IGMP support

TCP OFFLOAD ENGINE (TOE)
- Up to 8 TCP connections accessible to Host and User Logic
- Support up to 2K bytes Ethernet frames

USER LOGIC
- 8 dedicated DMA Channels to/from Host System at full PCIe speed
- 256KB of register access
- All TCP and UDP streams accessible
- Access to all physical ports

SOFTWARE API
- Multi DMA channel streaming (64 channels) with host dependent DMA buffer
- C based API (DLL/Shared library). Windows, Linux & FreeBSD (on request)

ON-BOARD SENSOR READINGS
- Current fbSmartNIC1.0 System status available in Software API
- Temperature with present minimum, maximum card operating temperature

ON-BOARD SENSOR READINGS (cont.)
- Link status
- TCP State information

STANDARD NIC full
- Standard NIC Support
- Configurable to all available ports running alongside TOE and UDP Engine
- Data path also accessible to User Logic

STATISTICS
- Statistics are based on a subset of RFC2819 RMON1
- Statistics are provided on a per second basis:
- Network counter: Number of Octet, CRC Align Errors, Undersize Packets, Oversize Packets, Jabbers, etc.

MONITOR CHANNELS
- All outgoing packet can be looped back to Host through PCIe for monitoring or logging purposes

TCP and UDP accelerated Trading Scenario

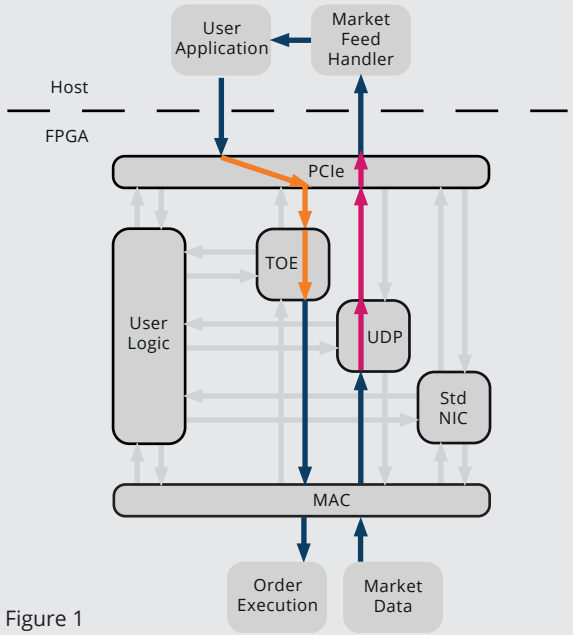

Figure 1

TCP and UDP accelerated Trading Scenario with MarketFeed Handler and Order Execution in User Logic

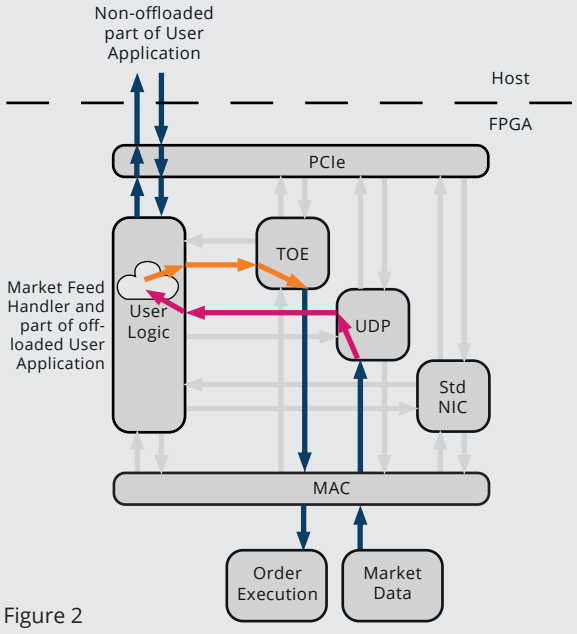

Figure 2

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